CLAIMS

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1. A receiver unit in a wireless communications system, comprising:

a first buffer operative to receive and store digitized samples at a particular sample rate; and

a data processor coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate.

2. The receiver unit of claim 1, further comprising:

a controller coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor.

3. The receiver unit of claim 2, wherein the controller is operative to direct processing of the segments of digitized samples.

4. The receiver unit of claim 2, wherein the controller is operative to perform pilot processing and time tracking for each signal instance being processed.

5. The receiver unit of claim 2, wherein the controller is operative to perform lock detection of each signal instance being processed.

6. The receiver unit of claim 2, wherein the controller is operative to perform frequency tracking of the digitized samples.

7. The receiver unit of claim 1, further comprising:

a receiver operative to receive and process a transmitted signal to provide the digitized samples.

8. The receiver unit of claim 1, wherein the data processor includes

a correlator operative to despread the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples.

9. The receiver unit of claim 8, wherein the data processor further includes

a symbol demodulation and combiner coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols.

10. The receiver unit of claim 8, wherein the data processor further includes

an accumulator coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results.

11. The receiver unit of claim 9, wherein the data processor further includes

a second buffer coupled to the symbol demodulation and combiner and operative to store the processed symbols.

12. The receiver unit of claim 8, wherein the correlator includes

a set of K multipliers operative to concurrently despread sets of up to K complex digitized samples.

13. The receiver unit of claim 12, wherein the correlator further includes

a set of K summers coupled to the set of K multipliers, each summer operative to receive and sum pairs of samples from two multipliers.

14. The receiver unit of claim 8, wherein the correlator includes

an interpolator operative to receive and interpolate despread samples from the PN despreading to generate interpolated samples that are provided as the correlated samples.

15. The receiver unit of claim 14, wherein the interpolator includes

one or more pairs of scaling elements, each scaling element operative to receive and scale respective despread samples with a particular gain to generate scaled samples, and

one or more summer, each summer coupled to a respective pair of scaling elements and operative to receive and sum the scaled samples from the pair of scaling elements to generate the interpolated samples.

16. The receiver unit of claim 9, wherein the symbol demodulation and combiner includes

a decover element operative to receive and decover the correlated samples with one or more channelization codes to provide decovered symbols.

17. The receiver unit of claim 16, wherein the channelization codes are Walsh codes having a length that is programmable and defined by the parameter values.

18. The receiver unit of claim 16, wherein the decover element is implemented with a fast Hadamard transform (FHT) element having L stages.

19. The receiver unit of claim 18, wherein the FHT element is operative to receive and process inphase and quadrature correlated samples on alternating clock cycles.

20. The receiver unit of claim 18, wherein the FHT element is operative to perform decovering with one or more Walsh symbols of a length of 1, 2, 4, 8, 16, 32, 64, or 128.

21. The receiver unit of claim 16, wherein the symbol demodulation and combiner further includes

a pilot demodulator coupled to the decover element and operative to demodulate the decovered symbols with pilot symbols to provide demodulated symbols.

22. The receiver unit of claim 21, wherein the symbol demodulation and combiner further includes

a symbol accumulator coupled to the pilot demodulation and operative to accumulate the demodulated symbols from multiple signal instances to provide the processed symbols.

23. The receiver unit of claim 11, wherein the second buffer is operative to provide the processed symbols to a subsequent signal processing element in an output order that is different from an input order to provide de-interleaving of the processed symbols.

24. The receiver unit of claim 23, wherein the second buffer includes at least two sections, one section operative to store processed symbols for a

current packet being processed and another section operative to store processed symbols for a prior processed packet to be provided to the subsequent signal processing element.

25. The receiver unit of claim 10, wherein the accumulator is operative to accumulate the correlated samples over a programmable time interval to provide pilot signal estimates.

26. The receiver unit of claim 10, wherein the accumulator includes a plurality of accumulate elements, each accumulate element operative to provide pilot signal estimate for a particular time offset.

27. The receiver unit of claim 2, wherein the controller is operative to instantiate a timing state machine for each signal instance being processed.

28. The receiver unit of claim 27, wherein each instantiated timing state machine includes

a time tracking loop operative to track movement of the signal instance being processed.

29. The receiver unit of claim 2, wherein the controller is operative to receive a timing signal and initiate processing of the segments of digitized samples in response to the received timing signal.

30. The receiver unit of claim 29, wherein the timing signal is generated based on a comparison value provided by the controller.

31. The receiver unit of claim 29, wherein the timing signal is indicative of a particular number of digitized samples having been stored to the first buffer.

32. The receiver unit of claim 2, wherein the sample rate is asynchronous with the processing clock, .

33. The receiver unit of claim 2, further comprising

a micro-controller coupled to the controller and operative to receive the dispatched tasks and to generate a set of control signals to direct the operation of the first buffer and the data processor to execute the dispatched tasks.

34. The receiver unit of claim 33, wherein the micro-controller is operative to instantiate a task state machine for each task being processed.

35. The receiver unit of claim 33, wherein the micro-controller includes

a set of latches operative to latch a dispatched task and one or more parameter values to be applied for the dispatched task,

at least one counter, each counter coupled to a respective latch and operative to provide an indicator signal based on a value stored in the latch, and

a sequencing controller operative to receive at least one indicator signal and the dispatched task and to generate the set of control signals.

36. The receiver unit of claim 1, further comprising:

a data interface coupled to the first buffer, the data interface operative to receive the digitized samples, discard unnecessary samples, and assemble the samples into words suitable for efficient storage to the first buffer.

37. The receiver unit of claim 1, wherein a word of 32 bits or more is written to the first buffer or read from the first buffer for each buffer access.

38. The receiver unit of claim 1, wherein the first buffer is operative to store two or more packets of digitized samples.

39. The receiver unit of claim 1, wherein the first buffer is further operative to store PN samples used for despreading the digitized samples.

40. The receiver unit of claim 1, wherein multiple instances of the received signal are processed by retrieving and processing segments of digitized samples at multiple time offsets.

41. The receiver unit of claim 1, wherein at least one of the parameter values is programmable.

42. The receiver unit of claim 1, wherein the sample rate is twice a chip rate of the communications system.

43. The receiver unit of claim 1, wherein the frequency of the processing clock is at least ten times higher than the sample rate.

44. The receiver unit of claim 1, wherein the wireless communications system is a high data rate (HDR) CDMA system.

45. A user terminal in a spread spectrum communications system comprising the receiver unit of claim 1.

46. A base station in a spread spectrum communications system comprising the receiver unit of claim 1.

47. A receiver unit in a wireless communications system, comprising:

a receiver operative to receive and process a transmitted signal to provide digitized samples at a particular sample rate;

a first buffer coupled to the receiver and operative to receive and store the digitized samples;

a data processor coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate, and wherein the data processor includes

a correlator operative to despread the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples,

a symbol demodulation and combiner coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols,

a second buffer coupled to the symbol demodulation and combiner and operative to store the processed symbols, and

an accumulator coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results; and

a controller coupled to the data processor and operative to dispatch tasks for the data processor and to process the accumulated results from the data processor.

48. A method for processing a received signal in a wireless communications system, the method comprising:

receiving, processing, and digitizing a transmitted signal to provide digitized samples at a particular sample rate;

buffering the digitized samples in a first buffer;

retrieving segments of digitized samples from in the first buffer; and

processing the retrieved segments with a particular set of parameter values, wherein the processing is performed based on a processing clock having a frequency that is higher than the sample rate.

49. The method of claim 48, wherein the processing includes despreading the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples.

50. The method of claim 49, wherein the processing further includes decovering the correlated samples with one or more channelization codes to provide decovered symbols.

51. The method of claim 50, wherein the processing further includes demodulating the decovered symbols with pilot symbols to provide demodulated symbols.

52. The method of claim 51, wherein the processing further includes accumulating the demodulated symbols from multiple signal instances to provide processed symbols.

53. The method of claim 48, wherein the sample rate is asynchronous with the processing clock, the method further comprising:

tracking a chip rate of the digitized samples; and

providing a signal used to write digitized samples to the first buffer starting at designated locations.

54. A method for processing a received signal in a wireless communications system, the method comprising:

receiving, processing, and digitizing a transmitted signal to provide digitized samples at a particular sample rate;

buffering the digitized samples in a first buffer;

retrieving segments of digitized samples from the first buffer;

processing the retrieved segments with a particular set of parameter values, wherein the processing is performed based on a processing clock having a frequency that is higher than the sample rate, and wherein the processing includes

despreading the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples,

decovering the correlated samples with one or more channelization codes to provide decovered symbols,

demodulating the decovered symbols with pilot symbols to provide demodulated symbols, and

accumulating the demodulated symbols from multiple signal instances to provide processed symbols.

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